Materials Science and Engineering Doctoral Defense

Capable Copper Electrodeposition Process for Integrated Circuit - Substrate Packaging Manufacturing

School for Engineering of Matter, Transport and Energy

Kousik Ganesan

Advisor: Dr. Amaneh Tasooji

abstract

In this work, a capable reverse pulse deposition methodology is demonstrated to influence gap fill behavior inside microvia along with a uniform deposit in the fine line patterned regions for substrate packaging applications. Interconnect circuitry in IC substrate packages comprises of stacked microvia that varies in depth from 20μm to 100μm with an aspect ratio of 0.5 to 1.5 and fine line patterns defined by photolithography. Photolithography defined pattern regions incorporate a wide variety of feature sizes including large circular pad structures with diameter of 20μm - 200μm, fine traces with varying widths of 3μm - 30μm and additional planar regions to define a IC substrate package. Electrodeposition of copper is performed to establish the desired circuit. Electrodeposition of copper in IC substrate applications holds certain unique challenges in that they require a low cost manufacturing process that enables a void free gap fill gap fill inside the microvia along with uniform deposition of copper on exposed patterned regions. Deposition time scales to establish the desired metal thickness for such packages could range from several minutes to few hours. In this work, we show case a reverse pulse electrodeposition methodology that achieves void free gap fill inside the microvia and uniform plating in FLS (Fine Lines and Spaces) regions with significantly higher deposition rates than traditional approaches. In order to achieve this capability, systematic experimental and simulation studies were performed to show a strong correlation of the independent parameters that govern the electrodeposition process such as bath temperature, reverse pulse plating parameters and the ratio of various electrolyte concentrations to the deposition kinetics and deposition uniformity in fine patterned regions and gap fill rate inside the microvia. Additionally, insight into the physics of via fill process is presented with secondary and tertiary current simulation efforts. Such efforts lead to show “smart” control of deposition rate at the top and bottom of the via to avoid void formation. Finally, a parametric effect on grain size and the ensuing copper metallurgical characteristics of bulk copper is also shown to enable high reliability substrate packages for the IC packaging industry.

February 9, 2018; 2:00 PM; ERC 490